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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,171	02/12/2004	Shin Su	12681-US-PA	2170

31561 7590 10/04/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,171	SU ET AL.	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

All claims include the limitations of "a substrate of first type," "region of second type," etc. The limitations of the "first type" and "second type" render the claims indefinite because it is not clear what these "types" refer to. For instance, it is uncertain whether the substrate is a "first conductivity type," a "first silicon type," a "first insulating type," a "first transparent type," etc. It is assumed that the limitations pertain to "conductivity types," however the limitations will have to be further defined so that it is clear what the applicant intends to recite as the claimed structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder (US 6,215,135 B1) in view of Chen et al. (US 6,016,002).

In re claim 1, Schroder shows (fig. 1) an electro-static discharge (ESD) protection circuit for a dual polarity input/output (I/O) pad, comprising: a substrate (SBSTR) of first type; a deep well region of second type (WLL) disposed in the substrate of first type; a first transistor (MP) disposed over the well region of first type, wherein the first transistor comprises a first gate (g2), a first source (d5) and a first drain (d4); a second transistor (MN) disposed over the substrate of first type, wherein the second transistor comprises a second gate (g1), a second source (d1) and a second drain (d2), wherein the second source is connected with the first drain (in same well WLL), and wherein the second source and the first drain is disposed in a portion of the second type deep well region and a portion of the first type substrate; a first doped region (d6) disposed in the well region and laterally adjacent to the first source (d5), wherein the first doped region, the first source and the first gate are electrically connected to an input pad (part of VDD); and a second doped region (d3), disposed in the substrate of first type and laterally adjacent to the second drain (d2), wherein the second doped region, the second drain and the second gate are electrically connected to an output pad (part of Vss). Schroder shows all of the elements of the claims except the well region of the first type disposed in the deep well region of the second type. Chen et al. shows (fig. 4) an ESD protection circuit for an SCR in which a well (100) of a second conductivity type is formed in a deep well (98) of a first conductivity type. The well of the second conductivity type being part of the improvement (as compared to prior art figure 2) provides an ESD

circuit in which a trigger voltage is automatically adjusted to different trigger voltage levels in response to power being applied to the circuit (col. 1, lines 55-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the deep well of Schroder by adding a second well of a second conductivity type as taught by Chen to provide an ESD protection device that can adjust to a different trigger voltage in response to power being applied.

In re claims 2-6, Schroder discloses (col. 2, lines 36-67) that the substrate is a p-type, the deep well of the second type is an n-type well region, and the transistor (MN) is an NMOS transistor. The dope regions comprise a p-type region. Chen shows (fig. 4) that the well region (100) of the first type is also a p-type well region.

In re claims 7 and 8, the combined invention of Schroder and Chen inherently performs the same function during a positive or negative electro-static current because the combined invention has the same structure and materials as the applicant's claimed invention.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ameraseker et al. (US 6,081,002), Ker et al. (US 6,498,357 B2), and Lee et al. (US 6,538,266 B2) also show ESD structures for input/output pads.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571)

272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
October 1, 2004

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800